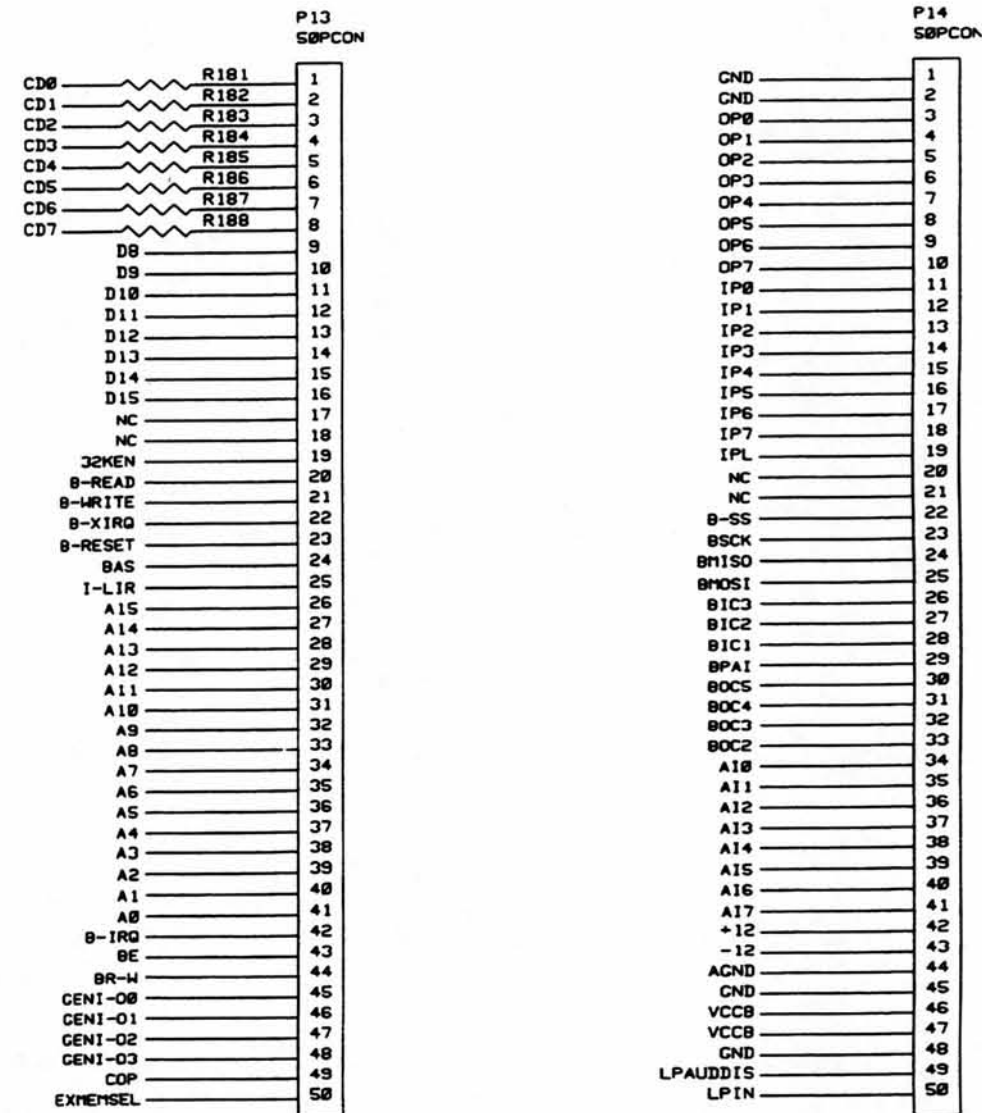
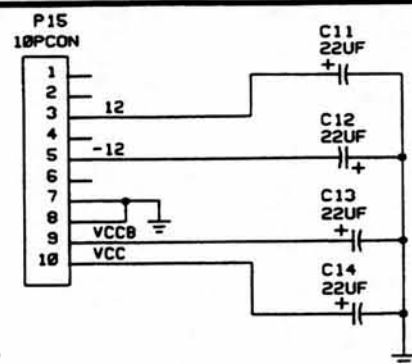


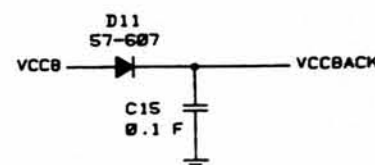
**SCHEMATIC #1**  
Trainer Power Supply Circuit Board



SIGNAL CONNECTOR BLOCKS



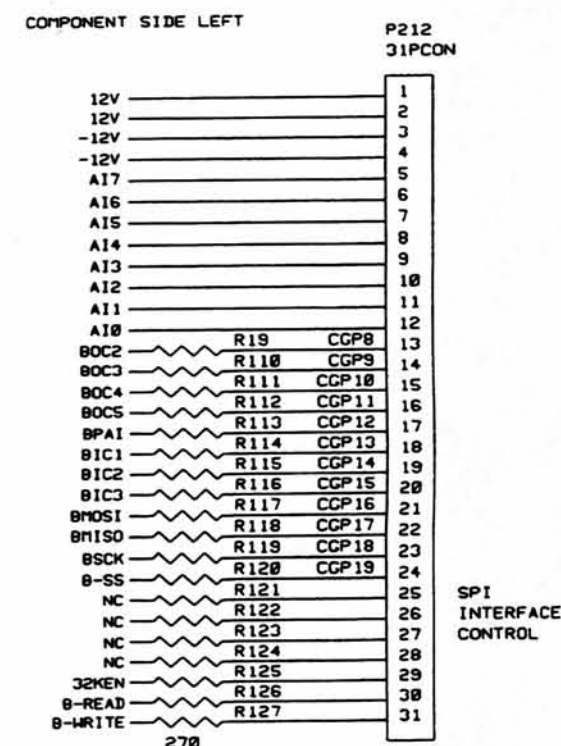
DC POWER IN



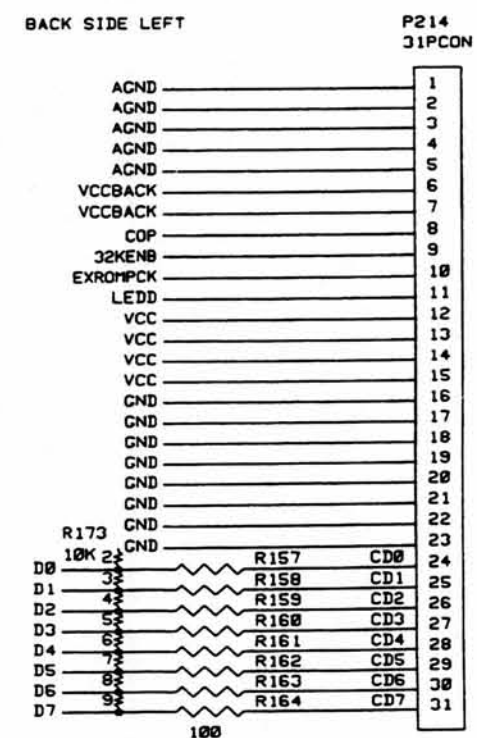
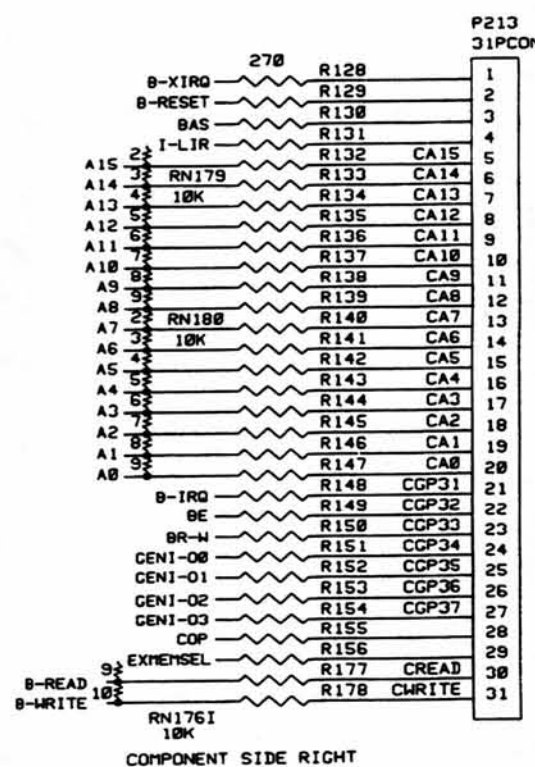
POWER NOTATION DEFINITION  
VCC- MAIN +5 VOLT SUPPLY  
VCCB- BREADBOARD +5 VOLT SUPPLY  
VCCA- ANALOG +5 VOLT SUPPLY

## SCHEMATIC #2

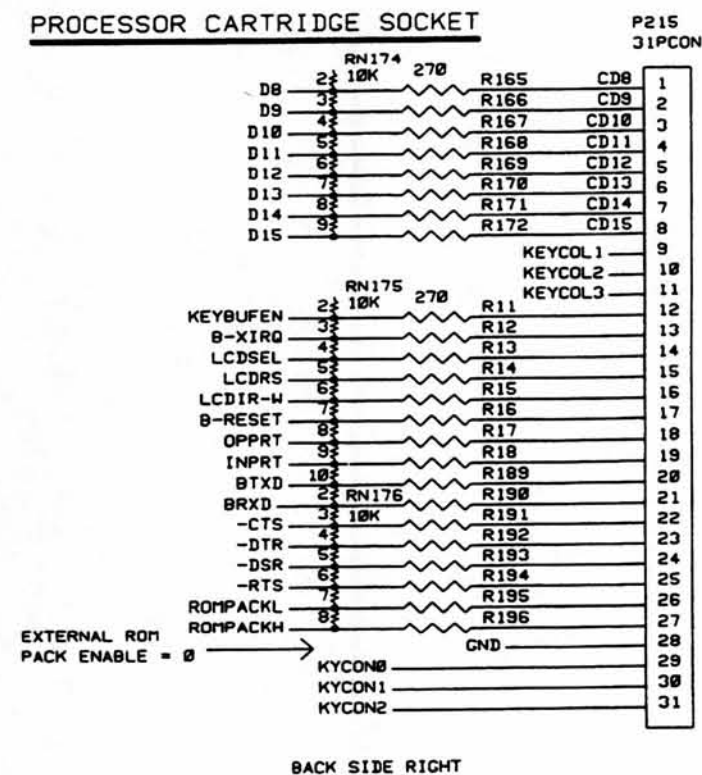
### Trainer

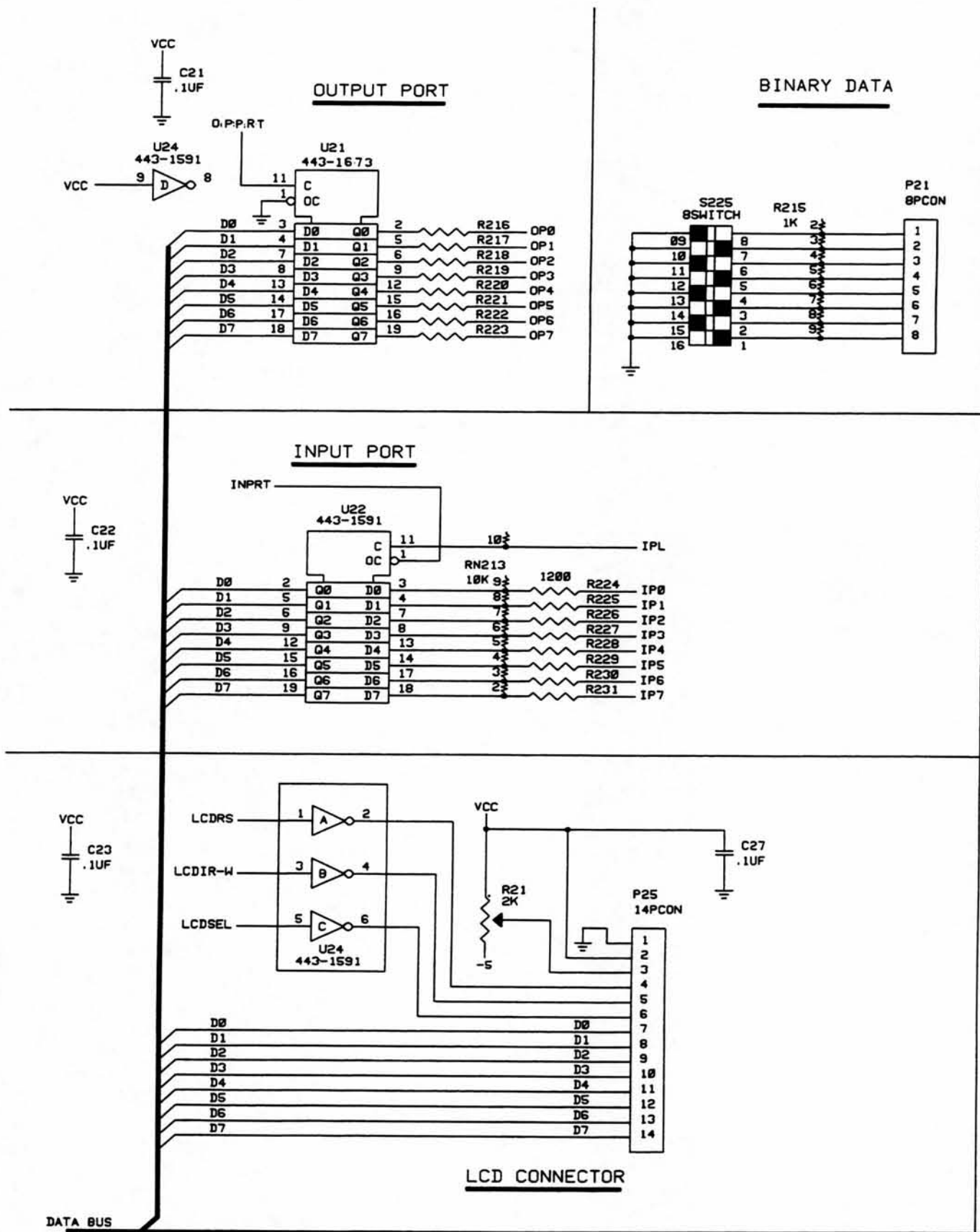


SPI INTERFACE CONTROL

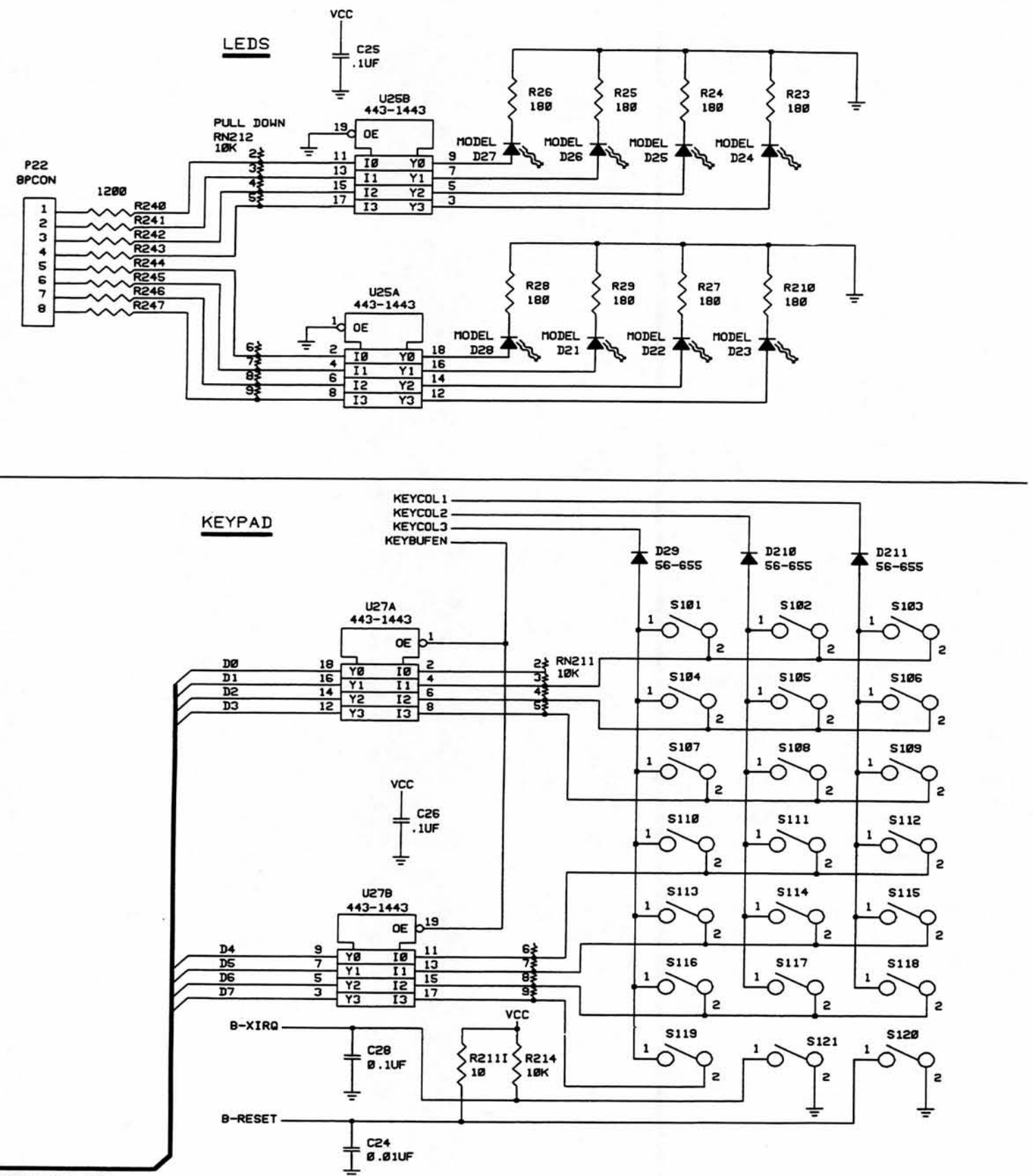


PROCESSOR CARTRIDGE SOCKET

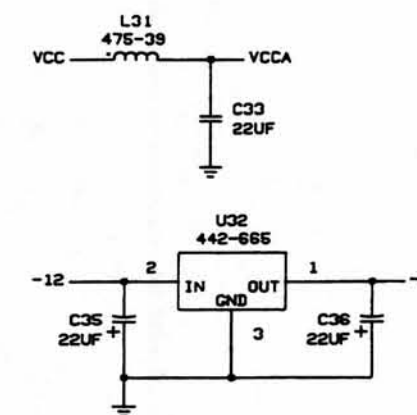




**SCHEMATIC #3**  
Trainer



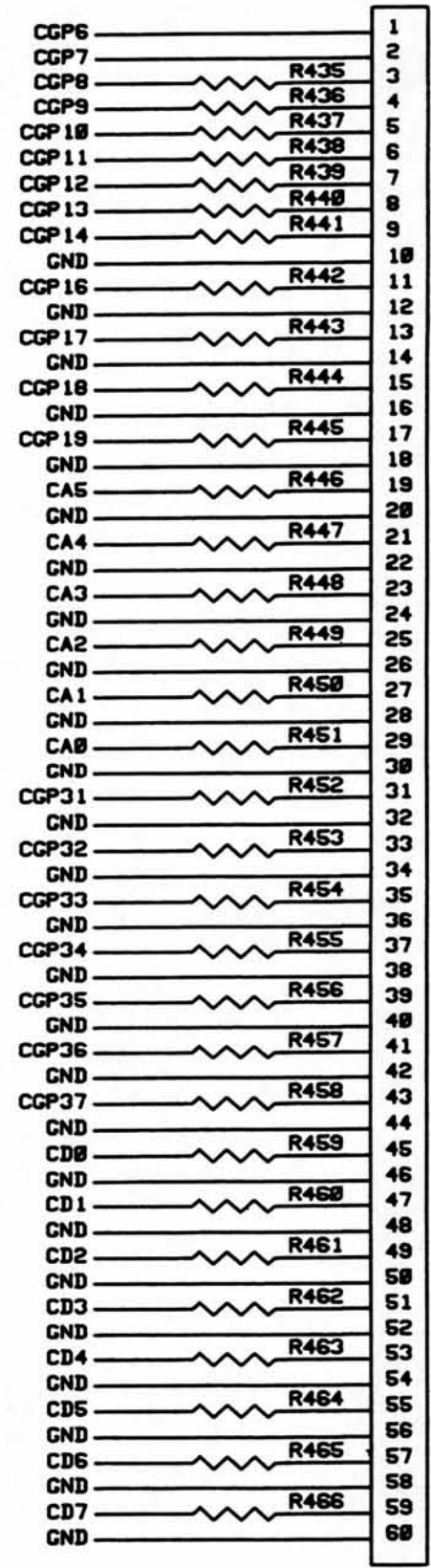
The diagram shows the internal wiring of an RS-232 interface. On the left, a U33 443-1467 driver chip contains six inverters labeled A through F. Each inverter's input is connected to a signal line: A to BTXD, B to BRXD, C to CTS, D to RTS, E to DTR, and F to DSR. The output of each inverter is connected to a corresponding pin on the P32 8PCON receiver chip. Specifically, inverter A connects to pin 8, B to pin 7, C to pin 6, D to pin 5, E to pin 4, and F to pin 3. Pin 1 of the P32 is connected to a common ground symbol. Pin 2 is connected to pin 12 (VDD), and pin 6 is connected to pin -12 (VSS). The P32 chip also has pins 3, 4, 5, 7, and 8, which are not connected in this diagram. To the right of the P32 chip is a vertical list of pin numbers: 6, 20, 7, 1, 2, 3, 4, 5, with an upward-pointing arrow next to the number 5. Above this list is the text 'External Connector pinout'.



Part of 595-4170-4

**BACKPACK CONNECTOR**

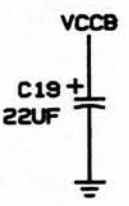
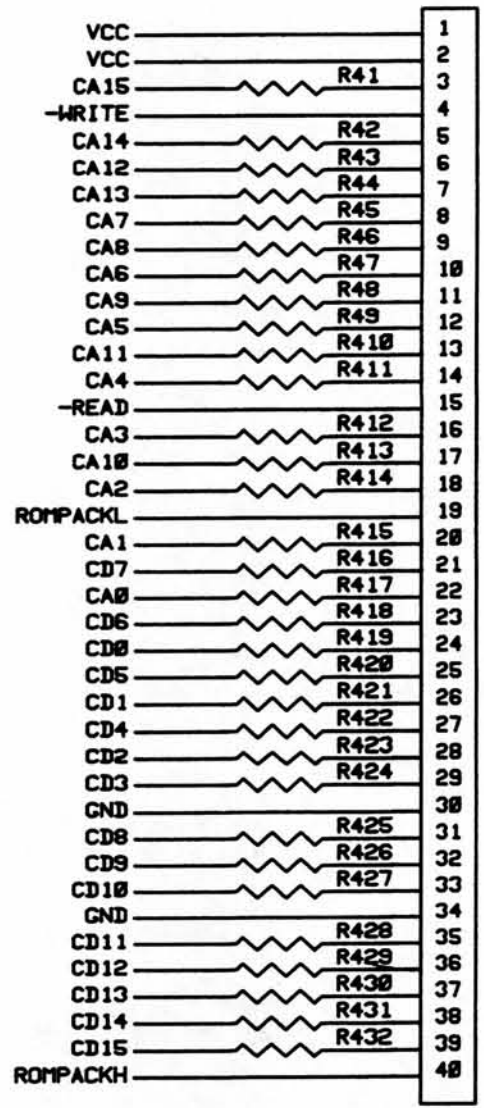
P11  
68PCON



**MEMORY CARTRIDGE**

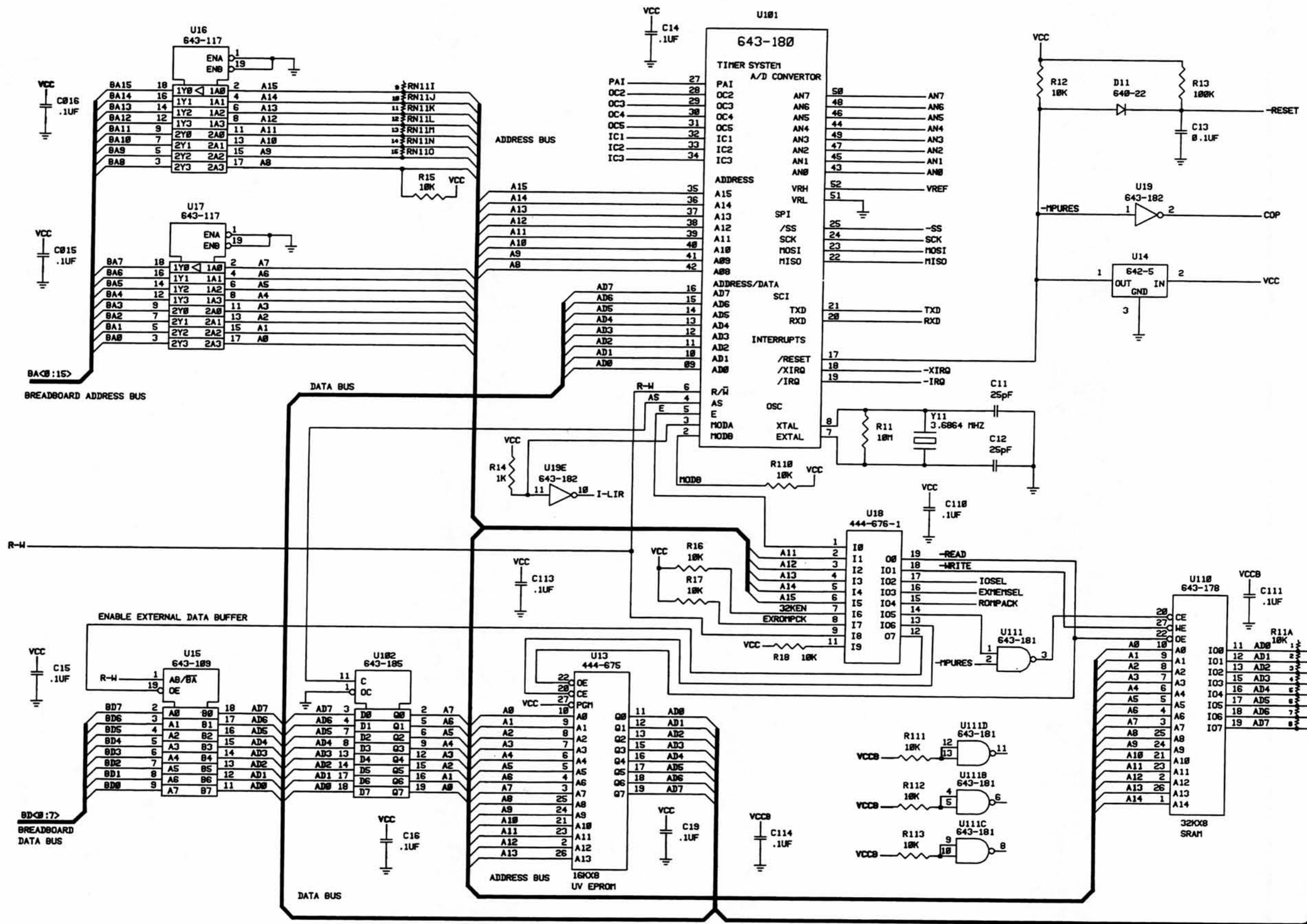
**SOCKET**

P12  
48PCON



**SCHEMATIC #5**  
Trainer





**SCHEMATIC #6**  
CPU Module

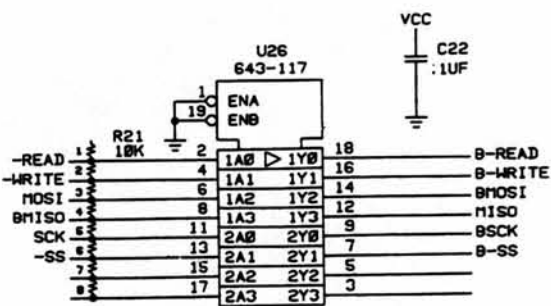
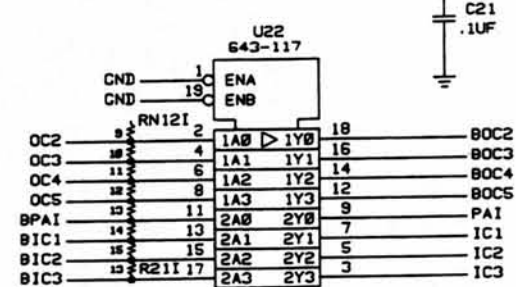
## I/O DECODING

ADDRESS MAP

Y0	0200H
Y1	0240H
Y2	0280H
Y3	02C0H
Y4	0300H
Y5	0340H
Y6	0380H
Y7	03C0H

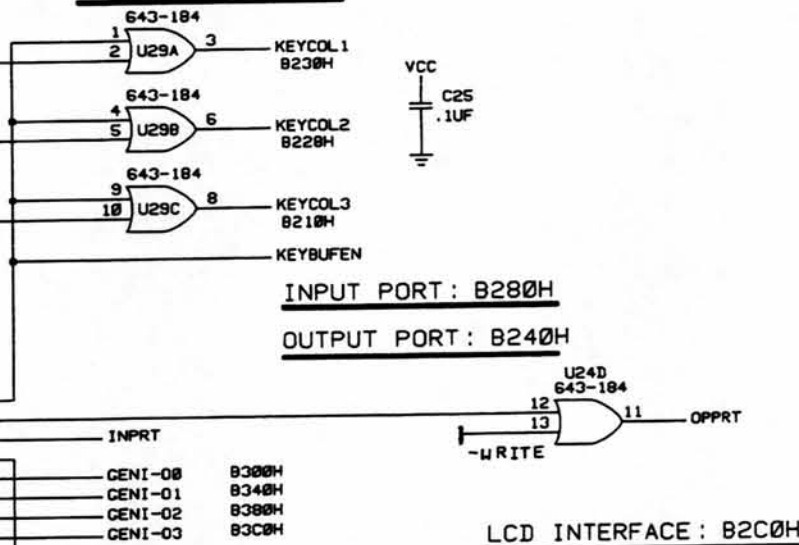
ADDRESS BUS

## TIMER SYSTEM BUFFER



## SERIAL PERIPHERAL INTERFACE BUFFER

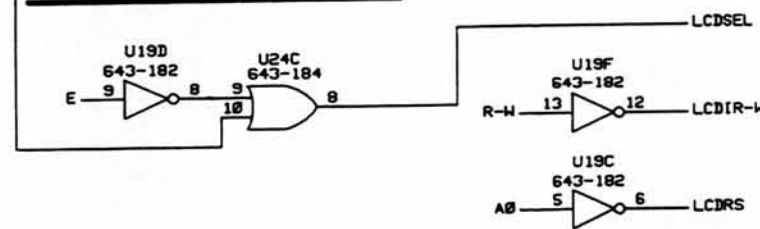
## KEYBOARD DECODING



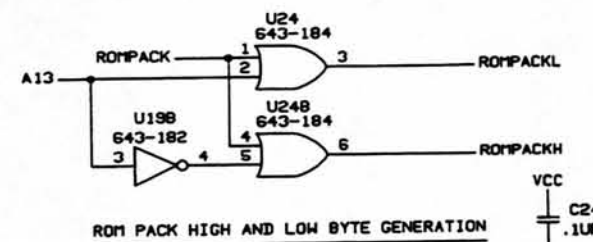
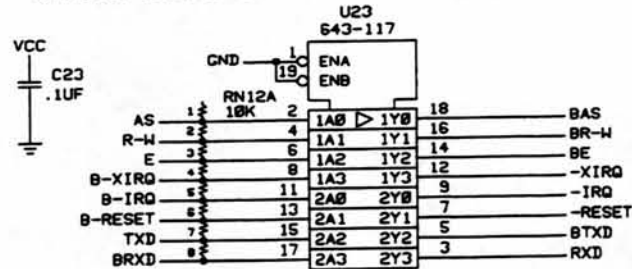
INPUT PORT: B280H

OUTPUT PORT: B240H

## GENERAL I/O SELECT LINES



## INTERRUPTS BUFFER SERIAL COMMUNICATION INTERFACE BUFFER



ROM PACK HIGH AND LOW BYTE GENERATION

## COMPONENT SIDE LEFT

12V	1
12V	2
-12V	3
-12V	4
A17	5
A16	6
A15	7
A14	8
A13	9
A12	10
A11	11
A10	12
B0C2	13
B0C3	14
B0C4	15
B0C5	16
BPA1	17
BIC1	18
BIC2	19
BIC3	20
BMOSI	21
BMISO	22
BSCK	23
B-SS	24
NC	25
NC	26
NC	27
NC	28
32KEN	29
B-READ	30
B-WRITE	31

## BACK SIDE LEFT

AGND	1
AGND	2
AGND	3
AGND	4
AGND	5
VCCB	6
VCCB	7
COP	8
32KENB	9
EXROMPCK	10
LEDD	11
VCC	12
VCC	13
VCC	14
VCC	15
CND	16
CND	17
CND	18
CND	19
CND	20
CND	21
CND	22
CND	23
CND	24
BD0	25
BD1	26
BD2	27
BD3	28
BD4	29
BD5	30
BD6	31
BD7	32

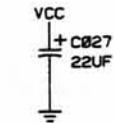
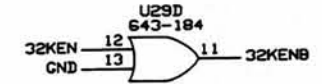
## EDGE BOARD CONNECTORS

## COMPONENT SIDE RIGHT

B-XIRQ	1
B-RESET	2
BAS	3
I-LIR	4
BA15	5
BA14	6
BA13	7
BA12	8
BA11	9
BA10	10
BA9	11
BA8	12
BA7	13
BA6	14
BA5	15
BA4	16
BA3	17
BA2	18
BA1	19
BA0	20
B-IRQ	21
BE	22
BR-W	23
GENI-00	24
GENI-01	25
GENI-02	26
GENI-03	27
COP	28
EXROMSEL	29
B-READ	30
B-WRITE	31

## BACK SIDE RIGHT

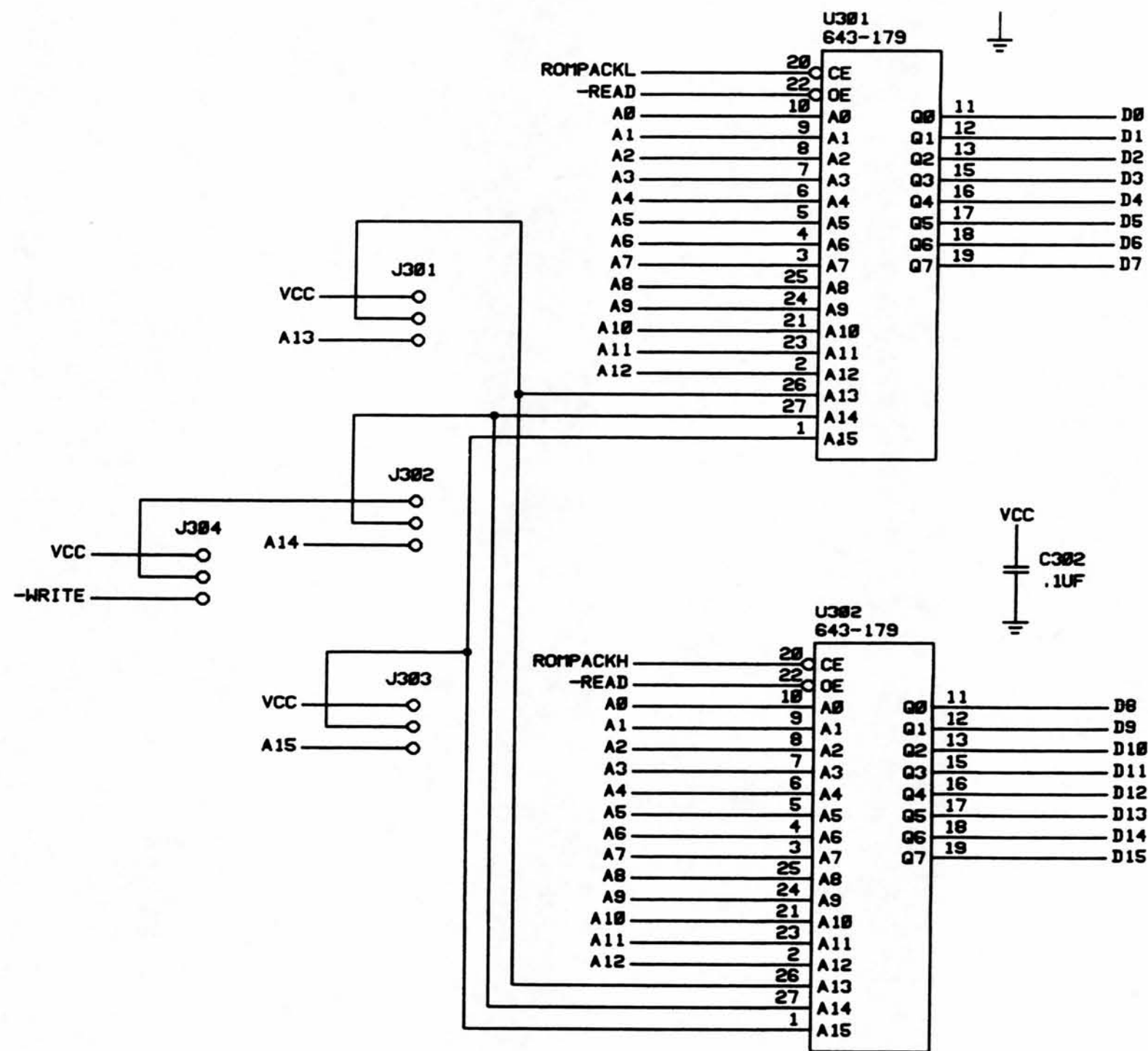
BD0	1
BD1	2
BD2	3
BD3	4
BD4	5
BD5	6
BD6	7
BD7	8
KEYCOL1	9
KEYCOL2	10
KEYCOL3	11
KEYBUFEN	12
B-XIRQ	13
LCDSEL	14
LCDIR-W	15
LCDRS	16
OPPR	17
INPR	18
BTXD	19
BRXD	20
NC	21
NC	22
NC	23
NC	24
NC	25
ROMPACKL	26
ROMPACKH	27
EXROMPCK	28
KYCON0	29
KYCON1	30
KYCON2	31



# SCHEMATIC #7 CPU Module







**SCHEMATIC #9**  
Memory Module

